



ZHEJIANG UNIU-NE Technology CO., LTD

浙江宇力微新能源科技有限公司



UNI2113S/P Data Sheet

V 1.1

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General Description

The UNI2113S/P are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Key Features

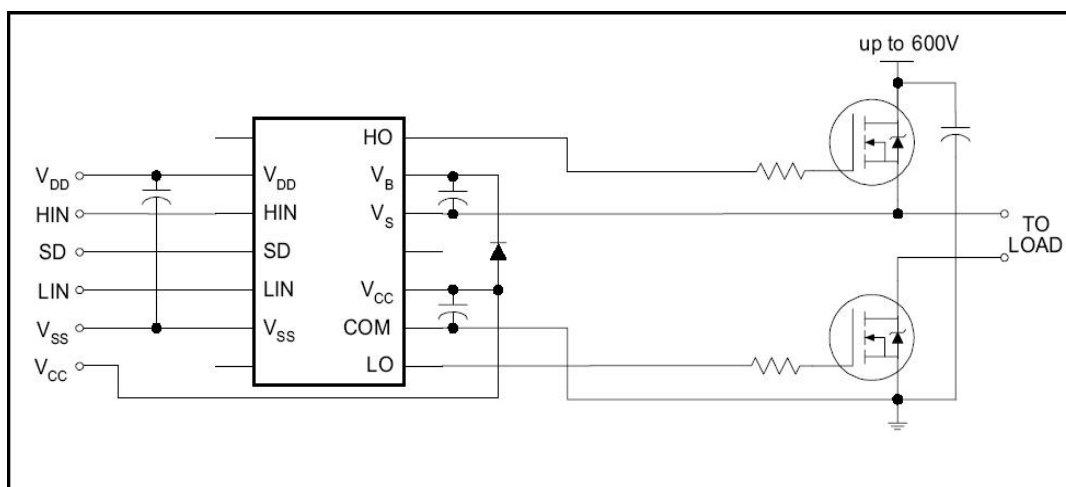
- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels

Applications

- Home appliances
- Industrial applications and drives
- Motor drivers
- DC, AC, PMDC and PMAC motors
- Induction heating
- HVAC

Typical Application

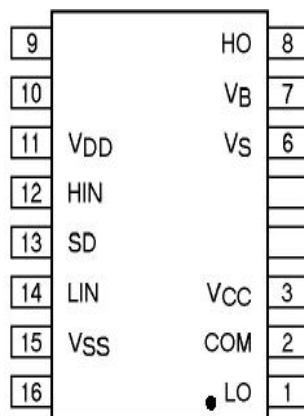
Typical application circuit using UNI2113S/P



Pin Assignments



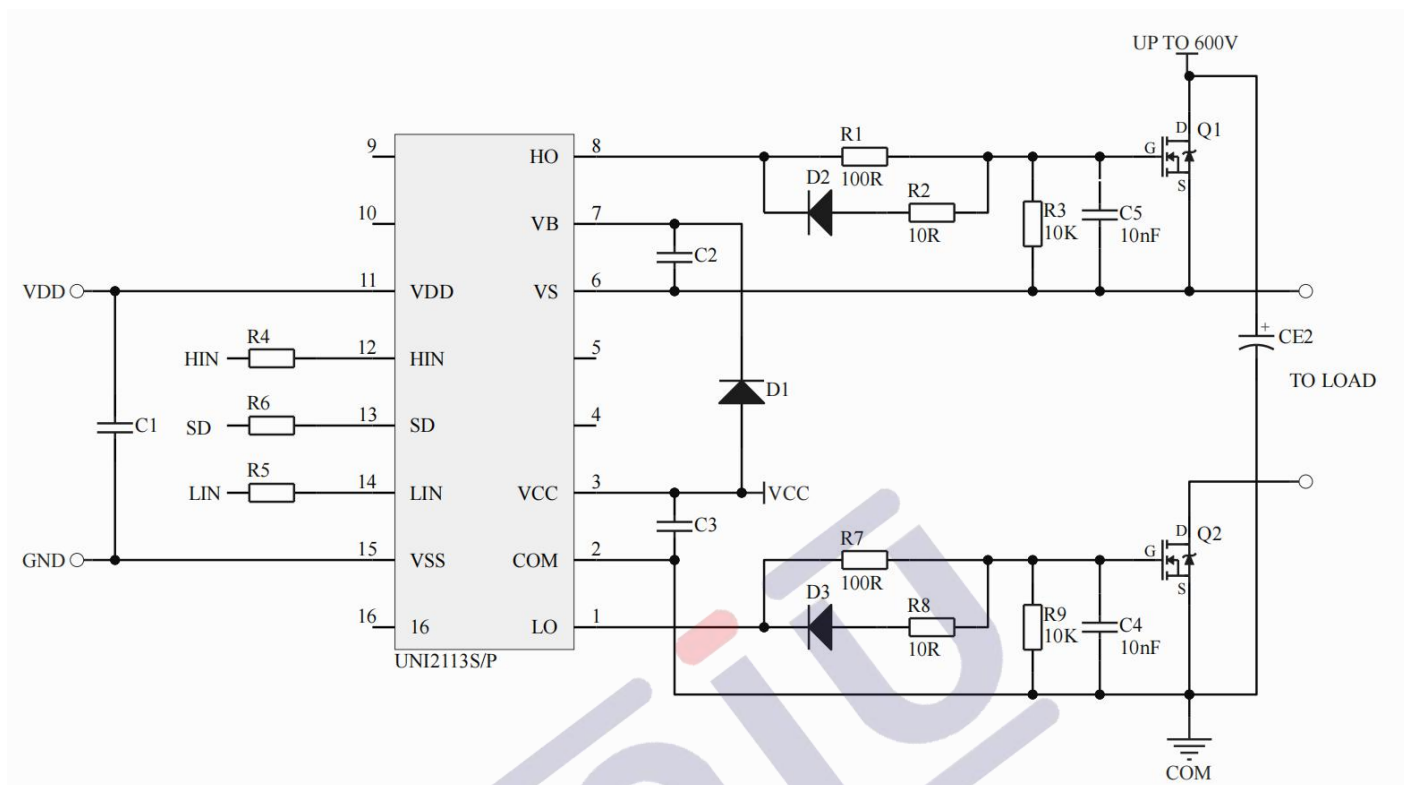
14 Lead PDIP

16 Lead SOIC
(Wide body)

Pin Function

Pin	Description
LO	Low side gate drive output
COM	Low side return
VCC	Low side supply
VS	High side floating supply return
VB	High side floating supply
HO	High side gate drive output
VDD	Logic supply
HIN	Logic input for high side gate driver out-put (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver out-put (LO), in phase
VSS	Logic ground

Typical Connection



1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2021/11/12	1.1	Layout adjustment

2.免责声明

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